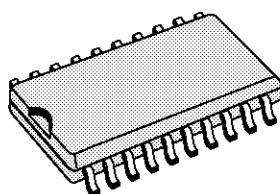


CONTROL HEAD PLAYBACK
 & RECORD AMPLIFIER AND SIGNALS INTERFACE

- CONTROL HEAD PLAYBACK AMPLIFIER WITH AGC
- CONTROL HEAD RECORD AMPLIFIER WITH SINK/SOURCE OUTPUT STAGE
- CONTROL PLAY-BACK SIGNAL INVERTER
- 4 COMPARATORS WITH INTERNAL FIXED THRESHOLD (2.5V)
- COMPARATORS WITH GROUND/V_S COMPATIBLE INPUTS AND OPEN COLLECTOR OUTPUTS


 SO20 LARGE
 (Plastic Micropackage)

ORDER CODE : TDA8118D

DESCRIPTION

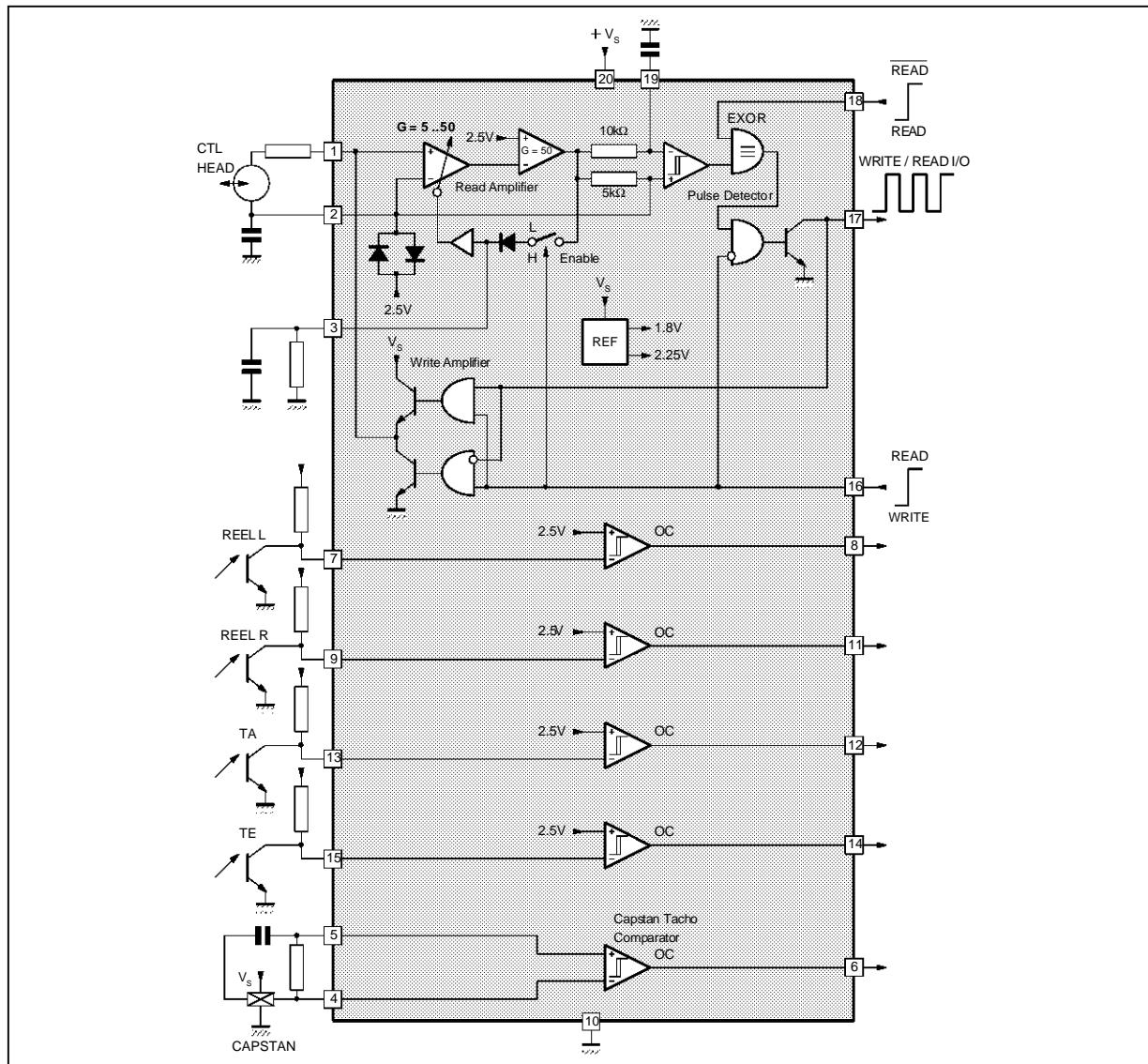
The TDA8118 is a bipolar integrated circuit for VCR application. It is intended to process the CTL-signal in record and playback mode. An internal AGC provides a wide range of input signal level. 5 further internal hysteresis comparators are intended to convert signals from optical and hall sensors to TTL-level.

PIN CONNECTIONS

CTL AMPLIFIER INPUT ; RECORD AMPLIFIER OUTPUT	<input type="checkbox"/>	1	<input type="checkbox"/>	20	V _S
CTL AMPLIFIER REFERENCE VOLTAGE	<input type="checkbox"/>	2	<input type="checkbox"/>	19	CTL READ AMPLIFIER FILTER OUTPUT
CTL AMPLIFIER AGC TIME CONSTANT	<input type="checkbox"/>	3	<input type="checkbox"/>	18	READ OUTPUT INVERTER
CAPSTAN TACHO COMPARATOR INVERTED INPUT	<input type="checkbox"/>	4	<input type="checkbox"/>	17	READ AMPLIFIER OC OUTPUT OR WRITE AMPLIFIER TTL COMPATIBLE INPUT
CAPSTAN TACHO COMPARATOR NOT INVERTED INPUT	<input type="checkbox"/>	5	<input type="checkbox"/>	16	READ / WRITE INPUT
CAPSTAN TACHO OPEN COLLECTOR OUTPUT	<input type="checkbox"/>	6	<input type="checkbox"/>	15	SENSOR INPUT
SENSOR INPUT	<input type="checkbox"/>	7	<input type="checkbox"/>	14	OPEN COLLECTOR SENSOR OUTPUT
OPEN COLLECTOR SENSOR OUTPUT	<input type="checkbox"/>	8	<input type="checkbox"/>	13	SENSOR INPUT
SENSOR INPUT	<input type="checkbox"/>	9	<input type="checkbox"/>	12	OPEN COLLECTOR SENSOR OUTPUT
GROUND	<input type="checkbox"/>	10	<input type="checkbox"/>	11	OPEN COLLECTOR SENSOR OUTPUT

TDA8118

BLOCK DIAGRAM



8118-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	DC Supply Voltage	14	V
V_i	DC Input Voltage	-0.3 to V_s	V
V_o	DC Output Voltage	V_s	V
I_o	Open Collector Output Current	5	mA
T_{stg}	Storage Temperature	-55 to 125	°C
T_j	Operating Junction Temperature	0 to 85	°C

8118-01.TBL

Note : The circuit is ESD protected according to MIL-STD-883C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

8118-02.TBL

ELECTRICAL CHARACTERISTICS $V_S = 5V \pm 5\%$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage (Pin 20)		4.5		6	V
I_S	Supply Current (Pin 20)	Pins 6, 8, 11, 12, 14, 16, 17 open			5	mA

CTL READ AMPLIFIER

V_{REF}	CTL Reference Voltage (Pin 2)		2.1	2.25	2.4	V
R_{IN}	Input Resistance (Pin 1)		100			kΩ
G_V	Voltage Gain (Pins 1/19)	AGC not active, Pin 3 = GND, $f = 1kHz$	66			dB
ΔG_V	Voltage Gain range of AGC (Pins 1/19)	$f = 1kHz$, $R_S = 220k\Omega$, $C_3 = 33\mu F$		18		dB
R_F	Filter Output Impedance (Pin 19)		7	10	13	kΩ
V_{IN}	Minimum Peak Input Voltage (Pin 1)		0.5			mV

CTL PULSE DETECTOR

I_{H+}	Positive Schmitt Trigger Threshold (Pins 17/19)	See timing diagram		$V_Z + 0.5$		V
I_{H-}	Negative Schmitt Trigger Threshold (Pins 17/19)	See timing diagram		$V_Z - 0.5$		V
V_{SAT}	Output Saturation Voltage (Pin 17)	$V_{17} = Low$, $I_{17} = 1.8mA$			0.4	V
I_C	Output Leakage Current (Pin 17)	$V_{17} = V_S$			10	μA
V_{REL}	Read Inverter Input Low Voltage (Pin 18)		-0.3		1.5	V
V_{REH}	Read Inverter Input High Voltage (Pin 18)		2.3		V_S	V

CTL WRITE AMPLIFIER

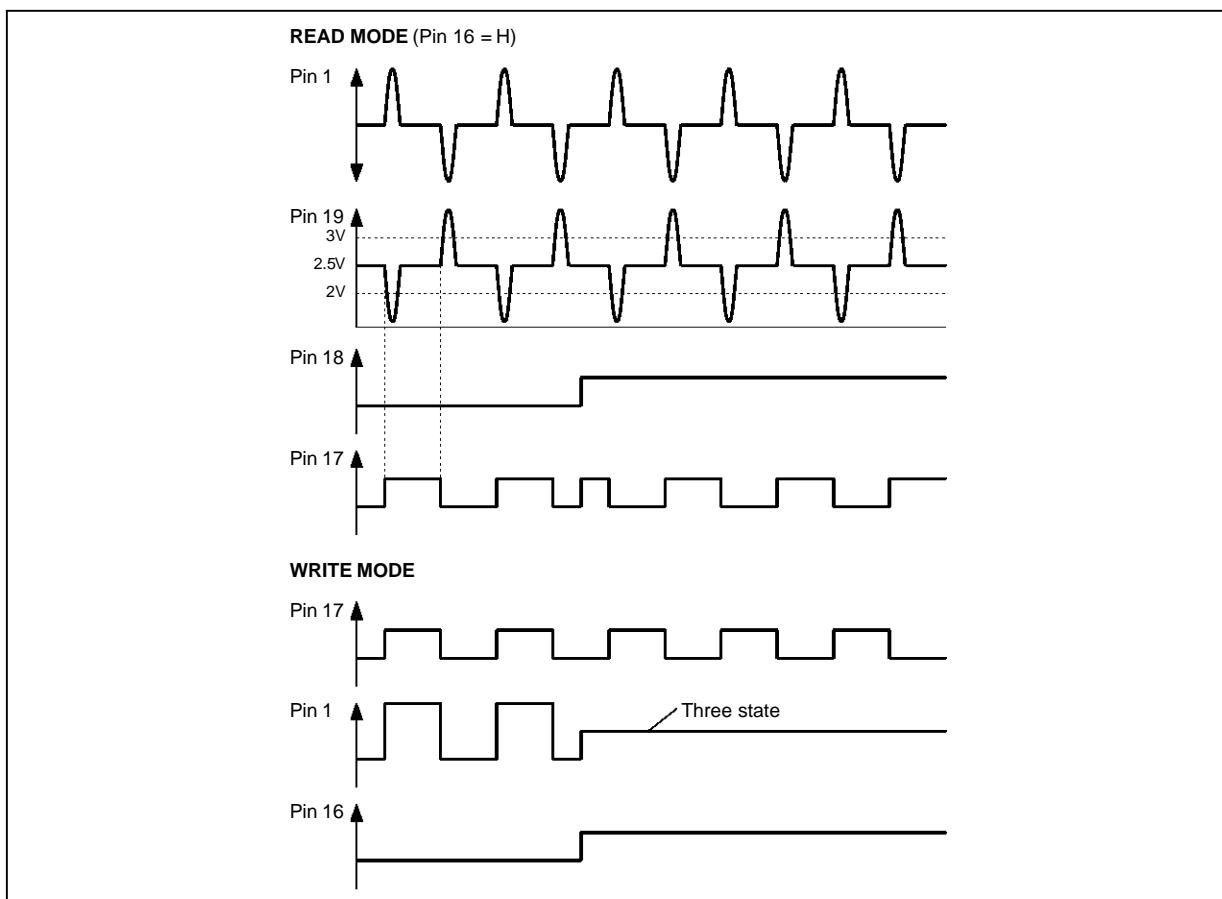
V_{RWL}	Read/Write Enable Input Low Voltage (Pin 16)		-0.3		1.5	V
V_{RWH}	Read/Write Enable Input High Voltage (Pin 16)		2.3		V_S	V
V_{WRL}	Write Input Low Voltage (Pin 17)	Pin 16 = Low	-0.3		1.5	V
V_{WRH}	Write Input High Voltage (Pin 17)	Pin 16 = Low	2.3		V_S	V
V_{SATL}	Output Saturation Voltage Low State (Pin 1)	$I_{SINK} = 5mA$, Pin 16 = Low, Pin 17 = Low			0.4	V
V_{SATH}	Output Saturation Voltage High State (Pin 1)	Pin 16 = Low, Pin 17 = High $I_{SOURCE} = 5mA$ $I_{SOURCE} = 2mA$			1.5 1.3	V

SENSOR INTERFACE

I_{IN}	Input Bias Current (Pins 7/9, 13/15)	$V_{IN} = 1V$	-3		1	μA
I_{TH}	Input Threshold Voltage (Pins 7/9, 13/15)		2.1	2.25	2.4	V
I_{HYS}	Input Hysteresis (Pins 7/9, 13/15)		150	200	250	mV
V_{SAT}	Output Saturation Voltage (Pins 8/11/12/14)	$I_{SINK} = 1.8mA$			0.4	V
I_L	Output Leakage Current (Pins 8/11/12/14)	$V_{OUT} = V_S$			10	μA

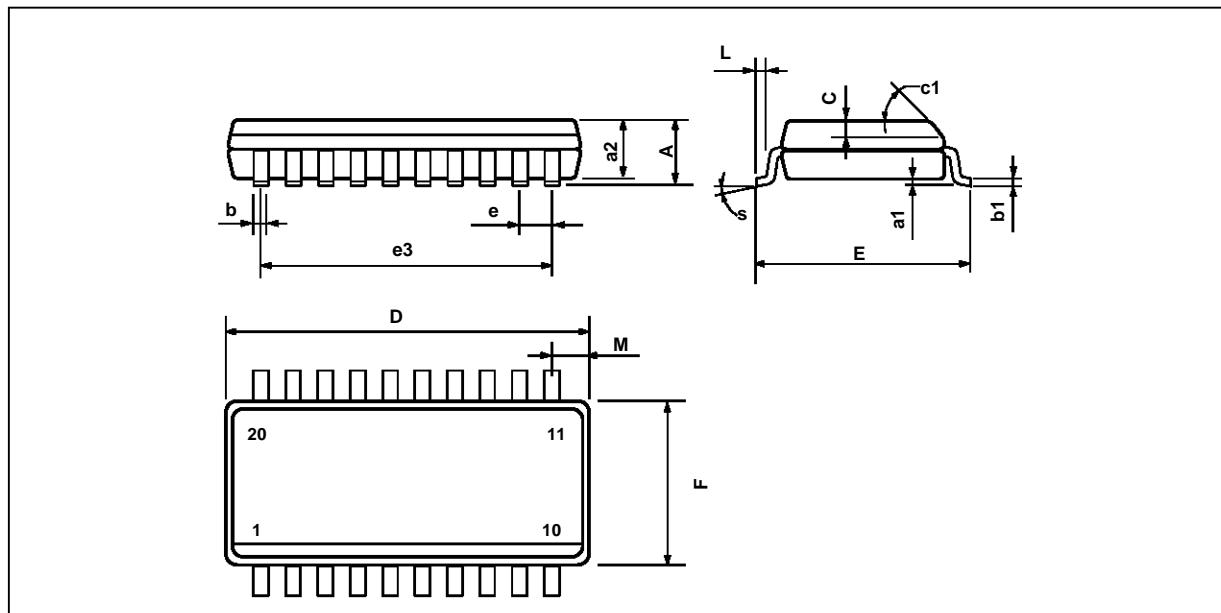
CAPSTAN TACHO COMPARATOR

I_{IN}	Input Bias Current (Pins 4/5)	$V_{IN} = Low$	-3		1	μA
V_{OFF}	Input Offset Voltage (Pins 4/5)				5	mV
I_{HYS}	Input Hysteresis (Pins 4/5)			5	10	mV
V_{SAT}	Output Saturation Voltage (Pin 6)	$I_{SINK} = 1.8mA$			0.4	V
I_{LEAK}	Output Leakage Current (Pin 6)	$V_{OUT} = V_S$			10	μA

TIMING DIAGRAM

8118-03.EPS

PACKAGE MECHANICAL DATA
20 PINS - PLASTIC MICROPACKAGE



PM-SO20L.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1			45° (typ.)			
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S			8° (max.)			

SO20L.EPS

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